CLAIMS

What is claimed is:

1. A method for monitoring prefetches due to speculative accesses in a computer system comprising:

providing a processor for processing data;

providing a cache memory, said cache memory capable of being accessed by said processor;

providing an off-chip memory system, said off-chip memory system capable of being accessed by said processor;

providing for speculative accesses by said processor to transfer data from said off-chip memory system to said cache memory system;

modifying said processor such that said processor is capable of determining and labeling accesses as speculative and said processor is capable of indicating to said cache memory whether an access is speculative or non-speculative;

providing said processor with a programmable prefetch counter that can be set, said prefetch counter for counting the number of prefetches, said prefetch counter providing said processor with the ability to trap on the occurrence of a predetermined state of said prefetch counter;

providing a bit per tag called an S-bit, said S-bit indicating whether a cache line was accessed speculatively, wherein;

a speculative insert of a cache line causes the S-bit of the cache line to be set, thereby changing the state of the cache line to the speculative state, further wherein;

a speculative update of a cache line results in the setting of the S-bit of the updated cache line,

thereby changing the state of the cache line to the speculative state, further wherein;

a speculative miss of a cache line results in no change, further wherein;

a non-speculative insert of a cache line results in the S-bit of the inserted cache line being cleared and the state of the cache line to be changed to the non-speculative state, further wherein;

a non-speculative update of a cache line results in incrementing the prefetch count of said programmable prefetch counter if the updated cache line S-bit is set and the clearing of the S-bit of the cache line to the non-speculative state, further wherein;

a non-speculative miss of a cache line results in no change.

2. The method for monitoring prefetches due to speculative accesses in a computer system of Claim 1, wherein;

said modifying said processor such that said processor is capable of determining and labeling accesses as speculative is accomplished by;

providing a cache address bus;

providing a bit line on said cache address bus to indicate whether an access is a speculative access.

3. The method for monitoring prefetches due to speculative accesses in a computer system of Claim 2, wherein;

modifying said processor such that said processor is capable of determining and labeling accesses as speculative is accomplished by providing said processor with a register that indicates what constitutes a speculative instruction.

4. A method for monitoring prefetches due to speculative accesses in a computer system comprising:

providing a processor for processing data;

providing a cache memory, said cache memory capable of being accessed by said processor;

providing an off-chip memory system, said off-chip memory system capable of being accessed by said processor;

providing for speculative accesses by said processor to transfer data from said off-chip memory system to said cache memory system;

modifying said processor such that said processor is capable of determining and labeling accesses as speculative and said processor is capable of indicating to said cache memory whether an access is speculative or non-speculative;

providing said processor with a programmable prefetch counter that can be set, said programmable prefetch counter for counting the number of prefetches, said programmable prefetch counter providing said processor with a table to hold instruction addresses called an instruction address table (IAT), wherein, the instruction address of a prefetched instruction is stored in the IAT;

providing said processor with the ability to trap according to a predetermined condition of said programmable prefetch counter, wherein, when a trap occurs a sample is taken from said prefetch occurrence that caused the trap;

providing a bit per tag called an S-bit, said S-bit indicating whether a cache line was accessed speculatively, wherein;

a speculative insert of a cache line causes the S-bit of the cache line to be set, thereby changing the state of the cache line to the speculative state, and the address to be stored, further wherein;

a speculative update of a cache line results in the setting of the S-bit of the updated cache line, thereby changing the state of the cache line to the speculative state, further wherein;

a speculative miss results in no change, further wherein;

a non-speculative insert of a cache line results in the S-bit of the inserted cache line being cleared, thereby changing the state of the cache line to the non-speculative state, further wherein;

a non-speculative update of a cache line results in incrementing the prefetch count of said programmable prefetch counter, the clearing of the S-bit if the updated cache line S-bit is set and, if said prefetch counter reaches said predetermined state and the present instruction caused the predetermined state, a trap is initiated, the address of the instruction that caused the trap is supplied from the IAT, and the data address of the prefetched cache line is supplied, further wherein;

a non-speculative miss results in no change.

5. The method for monitoring prefetches due to speculative accesses in a computer system of Claim 4, wherein;

said modifying said processor such that said processor is capable of determining and labeling accesses as speculative is accomplished by;

providing a cache address bus;

providing a bit line on said cache address bus to indicate whether an access is a speculative access.

6. A method for monitoring pollutions due to speculative accesses in a computer system comprising:

providing a processor for processing data;

providing a cache memory, said cache memory capable of being accessed by said processor;

providing an off-chip memory system, said off-chip memory system capable of being accessed by said processor;

providing for speculative accesses by said processor to transfer data from said off-chip memory system to said cache memory system;

modifying said processor such that said processor is capable of determining and labeling accesses as speculative and said processor is capable of indicating to said cache memory whether an access is speculative or non-speculative;

providing said processor with a programmable prefetch counter that can be set, said programmable prefetch counter for counting the number of prefetches, said programmable prefetch counter providing said processor with the ability to trap on the occurrence of a predetermined state of said prefetch counter;

providing a bit per tag called an S-bit, said S-bit indicating whether a cache line was accessed speculatively;

providing a bit per tag called an A-bit, said A-bit indicating whether a cache line was affected by a speculative access;

providing a table called an evicted tag table (ETT), said ETT containing one tag entry per cache set, entries in said ETT being used to store the most recently evicted cache line in the case that it was evicted because a speculative access occurred;

providing a pollution counter to count the number of pollutions;

providing instructions to read and clear said pollution counter;

modifying said processor such that said processor traps upon a predetermined state of said pollution counter, wherein;

a speculative insert of a cache line causes the S-bit of the cache line to be set, thereby changing the state of the cache line to the speculative state, the A-bit to be set of all other cache lines that do not have their S-bits set, thereby changing the state of all other cache lines that do not have their S-bits set to A-state, and the tag of the evicted cache line is moved to the ETT entry for this set, further wherein;

a speculative update of a cache line results in the setting of the S-bit of the updated cache line, thereby changing the state of the cache line from the non-speculative state to the speculative state and, if this access modifies the replacement ordering of the cache set, then the A-bits of all cache lines that had their replacement ordering modified are set and their S-bits are set to zero, further wherein;

a speculative miss of a cache line results in no change, further wherein;

a non-speculative insert of a cache line results in the S-bit of the inserted cache line being cleared and the state of the cache line being set to the non-speculative state and, if the evicted entry has the A-bit set, then the tag of the evicted cache line is moved to the ETT entry for the cache set, further wherein;

a non-speculative update of a cache line results in incrementing the prefetch count of said programmable prefetch counter if the updated cache line S-bit is set, the clearing of the S-bit, thereby changing the state of the cache line to the non-speculative state, clearing of the A-bit of all other cache lines, thereby changing the state of all other cache lines to the non-speculative state, and invalidating the ETT entry for this cache set, further wherein;

a non-speculative update of a cache line results in a change of state from the A-state to the non-speculative state, further wherein;

in the event of a non-speculative miss of a cache line, if the ETT entry for the set is valid and equals the tag of the accessed cache line, then the pollution count of said pollution counter is incremented and the ETT entry for this cache set is cleared.

7. The method for monitoring prefetches due to speculative accesses in a computer system of Claim 1, wherein;

said modifying said processor such that said processor is capable of determining and labeling accesses as speculative is accomplished by;

providing a cache address bus;

providing a bit line on said cache address bus to indicate whether an access is a speculative access.

8. The method for monitoring pollutions due to speculative accesses in a computer system of Claim 7, wherein;

modifying said processor such that said processor is capable of determining and labeling accesses as speculative is accomplished by providing said processor with a register that indicates what constitutes a speculative instruction.

9. A method for monitoring pollutions due to speculative accesses in a computer system comprising:

providing a processor for processing data;

providing a cache memory, said cache memory capable of being accessed by said processor;

providing an off-chip memory system, said off-chip memory system capable of being accessed by said processor;

providing for speculative accesses by said processor to transfer data form said off-chip memory system to said cache memory system;

modifying said processor such that said processor is capable of determining and labeling accesses as speculative and said processor is capable of indicating to said cache memory whether an access is speculative or non-speculative;

providing said processor with a programmable prefetch counter that can be set, said programmable prefetch counter for counting the number of prefetches, said programmable prefetch counter providing said processor with a table to hold instruction addresses called an instruction address table (IAT), wherein, the instruction address of a prefetched instruction is stored in the IAT;

providing said processor with the ability to trap on the occurrence of a predetermined state of said prefetch counter, wherein, when said prefetch counter reaches said predetermined state, a trap occurs and a sample is taken from said prefetch that caused said trap;

providing a bit per tag called an S-bit, said S-bit indicating whether a cache line was accessed speculatively;

providing a bit per tag called an A-bit, said A-bit indicating whether or not a cache line was affected by a speculative access;

providing a table called an evicted tag table (ETT), said ETT containing one tag entry per cache set, entries in said ETT being used to store the most recently evicted cache line in the case that it was evicted because a speculative access occurred;

providing a pollution counter to count the number of pollutions;

providing instructions to read and clear said pollution counter;

modifying said processor such that said processor traps upon said predetermined state of said pollution counter, wherein;

a speculative insert of a cache line causes the S-bit of the cache line to be set, thereby changing the state of the cache line to the speculative state, the A-bit to be set of all other cache lines that do not have their S-bits set, thereby changing the state of all other cache lines that do not have their S-bits set to A-state, the tag of the evicted cache line is moved to the ETT entry for the set and, the instruction address to be stored, further wherein;

a speculative update of a cache line results in the change of state from the A-state to the speculative state, further wherein;

a speculative update of a cache line results in the setting of the S-bit of the updated cache line, thereby changing the state of the cache line from the non-speculative state to the speculative state and, if the access modifies the replacement ordering of the cache set, then the A-bits of all cache lines that had their replacement ordering modified are set and their S-bits are set to zero, further wherein;

a speculative miss results in no change, further wherein;

a non-speculative insert of a cache line results in the S-bit of the inserted cache line being cleared, thereby changing the state of the cache line to the non-speculative state, and if the evicted entry has the A-bit set, then the tag of the evicted cache line is moved to the ETT entry for this cache set, further wherein;

a non-speculative update of a cache line results in incrementing the prefetch count of said programmable prefetch counter if the updated cache line S-bit is set, clearing the S-bit, thereby changing the state of the cache line to the non-speculative state, clearing

the A-bit of all other cache lines, thereby changing the state of all other cache lines to the non-speculative state, invalidating the ETT entry for this cache set, supplying the instruction address, and supplying the data address, further wherein;

a non-speculative update of a cache line results in a change of state from the A-state to the non-speculative state; and

a non-speculative miss of a cache line results in the pollution count of said pollution table being incremented, the ETT entry for the cache set being cleared, the instruction address being supplied, and the data address being supplied.

10. The method for monitoring prefetches due to speculative accesses in a computer system of Claim 9, wherein;

said modifying said processor such that said processor is capable of determining and labeling accesses as speculative is accomplished by;

providing a cache address bus;

providing a bit line on said cache address bus to indicate whether an access is a speculative access.